SCMOS2 Radiation Tolerant Technology Dual Port RAM 8Kx16 Tolerance to Radiation

by Thierry CORBIERE

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Abstract

This paper proposes a review of the data gathered during radiation testing for the 8Kx16 dual port RAM manufactured using the Radiation Tolerant version of the 0.6µm SCMOS2/2 technology. Both Upset sensitivity and Total Dose tolerance are assessed at 5.0V typical power supply. Effect of voltage reduction onto radiation tolerance is also measured at 3.3V. Latch-up immunity is verified at maximum LET of 123 MeV(mg/cm²).

Introduction

Introduction of any circuit to space grade requires deep investigation on its capability to operate in harsh environments. Presence of particles in the outer space imposes to characterize both the tolerance of the components against long term and cumulative ionization but also prompt deposition which occurs during particle travel across the silicon. Radioactive sources and particle accelerators are used to simulate effects on ground. Resulting data are then computerized to predict circuit degradation and event rates with respect to the satellite structure description and the environment models available from Space agencies.

Product Description

The double access port RAMs (DPR) manufactured using the radiation tolerant version of the MATRA MHS 0.6µm CMOS technology, offers interesting features for space engineers :

- Fast access time : 35/45/55 ns
- Wide temperature range : –55 °C to +125 °C
- Very low Stand-by current (400µA)
- Battery back-up operation : 2 V data retention
- TTL compatible
- Single 5 V ± 10 % power supply
- 3.3V data sheets available
- Full hardware support of semaphore signaling between ports
- Fully asynchronous operation from either port

Its 8 transistors cell (double access) has two benefits: it reduces the current through the cell (reduction of the power supply) but is also well adapted to noisy environments and prevents bit flips induced by local ionization (prompt effect), as for example heavy particle hit.

Space components manufactured with standard CMOS technology offer high speed, low consumption, very good long term reliability figures. But CMOS, in space, has a major drawback, particularly because of a SCR inherent structure which can, if trigged, induce low resistivity path between VDD and Ground. This is so called LATCH-UP and can be eliminated only if power supply is turned off. This phenomenon has catastrophic effect to space application and requires expensive countermeasures. The use of epitaxial starting material and adapted process technics can shift the level of LATCH-UP sensitivity far above from the level necessary for space application.

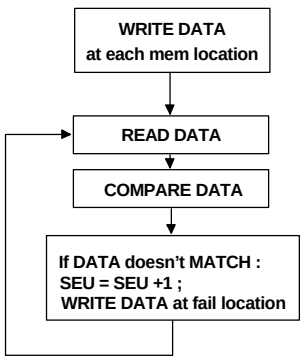
Ionization combined with high electrical field over oxide creates charge trapping with change in device characteristics as the basic active portion of MOS devices is oxide. Degradation rate is dependent on many parameters such as dose rate (dose at which the ionization is delivered), power supply and biasing during exposure, nature of the ionizing particle, etc... Radiation testing procedures impose the use of Cobalt 60 (1.17MeV gamma rays), ambient temperature irradiation and annealing sequence to assess the creation of post irradiation negative effects.

Heavy Ion Test Description

Test strategy consists into two major steps. First is the power supply current which is monitored during all the test sequences. Any major change in the typical value of this current informs the system a LATCH-UP occurs. A counter is increased when the supply current is turned off. Then, test starts again. Second, we measure the sensitivity of the cell to change content. This is controlled using the test sequence described in figure 1. Circuit is loaded with a reference pattern. Then, heavy ions come and the content of the memory is compared to the original pattern. Any error is reported and corrected. The two controls are repeated for any LET (Linear Energy Transfer) of interest.

Evaluation Report

figure 1 : Test Flow used during the heavy ions tests



Total Dose Test Description

According to the requirements of the applicable test procedures (ESA/SCC 22900 & MIL STD 883, TM1019.4), irradiation are conducted with ^{60}Co at ambient temperature. Devices are biased according to the schematic proposed in fig 2. Note that static levels are applied to the product during exposure.

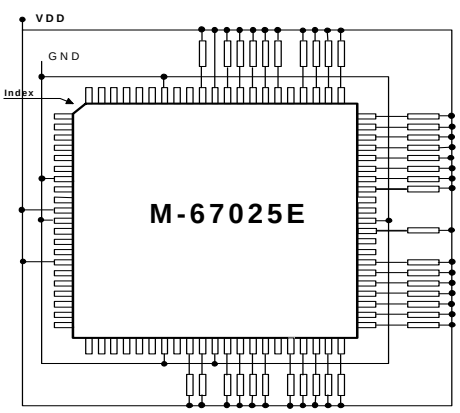


figure 2 : Bias used during total dose tests

Tested Components

The parts used for the purpose of this evaluation come from various lots manufactured since 94. They have been selected randomly after die sawing. Table 2 lists wafer lot numbers, their period of manufacturing and test. At minimum, electrical conformance against data sheet is verified before irradiation testing. Parts are mounted in Pin Grid Array 84 pins package (PGA).

During upset measurement, in order to not reduce the effectiveness of the particles, metallic cap is removed.

Lot	Format (BIT)	Qty	Date Code	Test Type	Dose max [Krad(Si)]
W29915	8K*16	9	9 532	Dose	70
W29915	8K*16	5	9 532	Ion	-
Z02131	8K*16	10	9 603	Dose	60
Z02131	8K*16	2	9 532	Ion	-

Table 1 : Devices used during radiation testing

Heavy Ion Test Results

IPN testing concerns more the UPSET sensitivity. This is why we selected cocktail of ions necessary to cover the 4 to 36MeV/(mg/cm²) range. For the remaining LATCH-UP sensitivity testing, Brookhaven, USA has been used. In that case, higher portion of the LET range is chosen (82.3 MeV/(mg/cm²). Table 2 gives the characteristics of the ions used during these two tests [2][3]. Note that Cosine law is used to vary LET of the particle (LET_{eff} = LET/Cos(@) with @=angle from particle to Silicon).

Ion	Energy (MeV)	LET [Mev/(mg/cm^2)]	Range in Si (µm)
19F	103	4,2	76
35Cl	154	12,7	45
79Br	196	36	30
197Au	352	82,3	27,9

Table 2 : Species used at IPN & BROOKHAVEN

First, no Latch-up is observed at maximum of LET tested (123 MeV/mg/cm²) [2]. Cross section per bit is less than 1E-7 cm². It means that, for space application, no occurrence of this catastrophic phenomenon will occur.
Table 3 lists the results obtained for memory cells tested at 5V. The figure 3 gives the evolution of the memory cell cross section per bit (versus the LET of the incident particle) observed during the IPN campaign. The cross section τ is calculated by using :

$$\tau = \frac{QTYEVENTS}{FLUENCE * COS(\Theta)} \qquad [1]$$

When the quantity of event is 0, then the calculation of the cross section τ uses 1 as default. The LET is expressed in [MeV/(mg/cm²)].

LETeff	Fluence$_{eff}$ (p/cm²)	upset	Cross Section / bit (cm²)
6	1 018 685	1	3.00E-11
7	538 256	22	1.25E-09
8	1 197 000	841	2.1E-08
12	1 709 500	8 005	1.43E-07
17,9	666 455	5 259	2.41E-07
24	166 744	10 305	1.89E-6
36	167 800	777	1.41E-07
36	2 113 332	1 600	2.31E-08

Table 3: SEU test results under 5V

	Irradiation [Krad(Si)]					Anneal (Hours)
Param	0	12.2	23.3	34.5	50	168
ICCOP (A)	0,21	0,21	0,21	0,21	0,21	0,19
ICCPD (µA)	47	47	152	102	3 800	3 200
ICC (mA)	2,56	2,56	2,64	2,6	50	7,4
IIL (µA)	0.0035	0.0035	0.0035	0	-0.011	0
IIH (µA)	-00071	-00071	0	0	-00071	0
VIL (V)	1,45	1,45	1,28	1,44	1,27	1,28
VIH (V)	1,52	1,52	1,8	1,52	1,78	1,78
VOL (%)	0	0	20	0	20	26
VOH (%)	0	0	-6	-1	-7	-11
TAVAV(nS)	19,3	19,3	19,5	19,4	18,9	19,2

Table 4: Total dose test results

Remarkable values are :

- *SEU LET threshold is 7 MeV/(mg/cm²)*
- *Saturation cross section / bit = 1.5E-07 cm²*

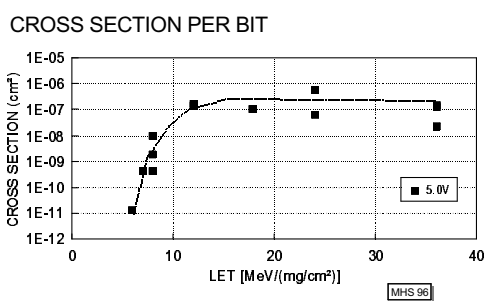


Figure 3: UPSET cross section / BIT = f(LET)

No functional failure occurs during the whole test sequence. The figure 4 illustrates the evolution of the power stand by current.

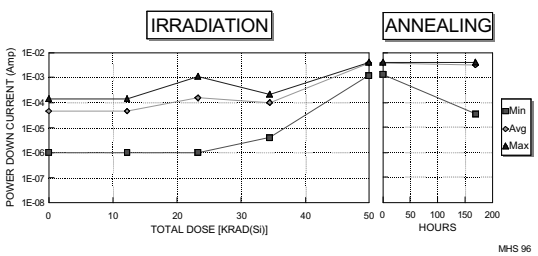


Figure 4: Stand-by current drift during and after irradiation

Total Dose Test Results

We will report only results gathered during the exposure up to 50Krad(Si) at 10Krad(Si)/h. Table 4 gives the average of measures extracted from the irradiation performed on the wafer lot n° W29915 [4]. Only parameter sensitive to ionization is reported. Last column of the table report the results during annealing sequence (168h at 100°C).

Sensitivity To Dose Rate

Current radiation norms impose dose rates far above the actual outer space. When some Krad per year are encountered by space missions, total dose procedures advise tens to hundreds Krad per hour. Many studies of the degradation dependency to dose rate have been conducted. Major outcome of one European Study [5] is proposed here under. The basic idea is that charge trapping can be extrapolated thanks to Arhenius law and energy of activation of the trapping phenomenon. Thus, starting from one irradiation conducted at high dose rate followed by various temperature/duration annealings, the degradation at very low dose rate is computerized.
Figure 4 illustrates the evolution of the power down current versus dose rate after 40Krad(Si) exposure for a FIFO manufactured with a similar CMOS RT technology.

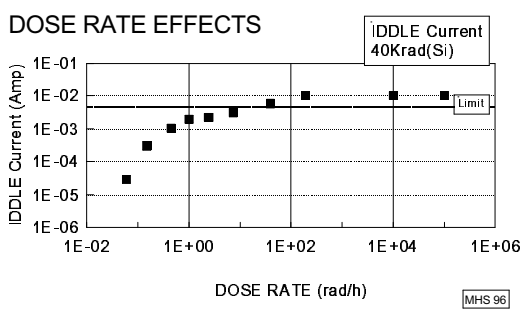


Figure 4: Effect of dose rate on supply current at 40Krad(Si)

After 40Krad(Si) exposure, more than 3 orders of magnitude lower degradation is expected at dose rate close to normal space environment compared to those imposed by the test procedures.

Additional Testing

Reduction of the power consumption required by the airborne applications while keeping highest level of performance requires to decrease the power supply voltage down to typically 3.3V. Ability of the product to work properly at 3.3V encourage to characterize also the Upset performance of the memory. Figure 5 depicts the difference between 5 and 3.3V SEU behavior for the first portion (lower values) of the LET spectra. Globally, the SEU threshold is reduced from 7 to 5 MeV/(mg/cm²) and the saturation cross section is increased by a factor of 2.

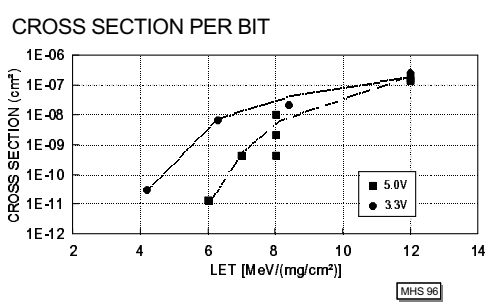


Figure 5: Variation of SEU sensitivity for 5 & 3.3V operation

Conclusions

Evaluation of the radiation hardness of the Dual Port RAM manufactured using the radiation tolerant version of 0.6µm CMOS technology has been satisfactorily conducted.

Heavy ion sensitivity has been assessed using two accelerators and the total dose tolerance of the products has been evaluated through numerous tests. The DPR family has very promising characteristics which are summarized here under :

- No LATCH-UP at 123 MeV/(mg/cm²) with a cross section below 1.0 E-07 cm²
- UPSET LET threshold at 7 MeV/(mg/cm²) with a saturation cross section per BIT at 1.5E-7 cm² for a 5 Volts power supply.
- UPSET sensitivity reduced at 5 MeV/(mg/cm²) when used at 3.3V with a cross section at 3E-7 cm²/bit..
- Functionality OK after 50Krad(Si) exposure with 10Krad(Si)/hour.
- Acceptable drift of the stand-by current after 35Krad(Si).
- Increased total dose tolerance when used in normal outer space environment because of its high dose rate sensitivity.

References

[1] "Hardening of the 0.6µm CMOS technology for Space Application", CNES contract n°844/93/0896/00, February 94

[2] "Resultats SEU/SEL", ONERA/CERT/DERTS, fax dated 31/05/96

[3] "Evaluation d'une Technologie à Divers Niveaux de Durcissement", ONERA/CERT/DERTS, report 448600 December 94.

[4] "Caracterisation de la technologie SCMOS2 RT", MATRA MHS, NT94055, December 94

[5] "WORK PACKAGE 5, final report", ESA contract n° 9849/92/NL, October 95.